CMOS Digital Integrated Circuits

Lec 2
Fabrication of MOSFETs
Categories of Materials

Materials can be categorized into three main groups regarding their electrical conduction properties:

- **Insulators**
- **Conductors**
- **Semiconductors**
While there are numerous semiconductor materials available, by far the most popular material is **Silicon**.

GaAs, InP and SiGe are compound semiconductors that are used in specialized devices.

The success of a semiconductor material depends on how easy it is to process and how well it allows reliable high-volume fabrication.
Single Crystal Growth

Pure silicon is melted in a pot (1400°C) and a small seed containing the desired crystal orientation is inserted into molten silicon and slowly (1mm/minute) pulled out.
Single Crystal Growth

The silicon crystal (in some cases also containing doping) is manufactured (pulled) as a cylinder with a diameter of 8-12 inches.

This cylinder is carefully sawed into thin disks (wafers). The wafers are later polished and marked for crystal orientation.
An IC consists of several layers of material that are manufactured in successive steps.

**Lithography** is used to selectively process the layers, where the 2-D mask geometry is copied on the surface.
Lithography

The surface of the wafer is coated with a photosensitive material, the **photoresist**. The mask pattern is developed on the photoresist, with UV light exposure.

Depending on the type of the photoresist (negative or positive), the exposed or unexposed parts of the photoresist change their property and become resistant to certain types of solvents.

Subsequent processing steps remove the undeveloped photoresist from the wafer. The developed pattern (usually) protects the underlying layer from an etching process. The photoresist is removed after patterning on the lower layer is completed.
Etching

Etching is a common process to pattern material on the surface. Once the desired shape is patterned with photoresist, the unprotected areas are etched away, using wet or dry etch techniques.
Patterning of Features on SiO$_2$

(a) Si -substrate

(b) SiO$_2$(Oxide)

(c) Photoresist

(d) Glass mask with feature

UV - Light

Insoluble photoresist

Soluble photoresist

SiO$_2$(Oxide)

Si -substrate

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Patterning of Features on SiO₂

1. Chemical etch (HF acid) or dry etch (plasma)
2. Hardened photoresist
3. SiO₂(Oxide)
4. Si -substrate

(e)

(f)

(g)
Oxide Growth / Oxide Deposition

Oxidation of the silicon surface creates a $\text{SiO}_2$ layer that acts as an insulator. Oxide layers are also used to isolate metal interconnections.

An annealing step is required to restore the crystal structure after thermal oxidation.
Ion Implantation

Ion implantation is used to add doping materials to change the electrical characteristics of silicon locally. The dopant ions penetrate the surface, with a penetration depth that is proportional to their kinetic energy.
Thin Film Deposition

While some of the structures can be grown on silicon substrate, most of the other materials (especially metal and oxide) need to be deposited on the surface.

In most cases, the material that is deposited on the whole surface will be patterned and selectively etched.

There are two main methods for thin film deposition:

- PVD  Physical Vapor Deposition
- CVD Chemical Vapor Deposition
Fabrication of nMOS Transistor

(a) Si - substrate

(b) SiO₂ (Oxide)

(c) SiO₂ (Oxide)

(d) Thin oxide, SiO₂ (Oxide)

Si - substrate
Fabrication of nMOS Transistor
Fabrication of nMOS Transistor

(h) Polysilicon

SiO$_2$ (Oxide) → n+ n+
Si - substrate

(i) Insulating oxide

SiO$_2$ (Oxide) → n+ n+
Si - substrate

(j) Insulating oxide

SiO$_2$ (Oxide) → n+ n+
Si - substrate
Fabrication of nMOS Transistor

Metal (Al)

SiO₂ (Oxide)

n+

n+

Si - substrate

Metal contact

SiO₂ (Oxide)

n+

n+

Si - substrate
CMOS Process

The CMOS process allows fabrication of nMOS and pMOS transistors side-by-side on the same Silicon substrate.
CMOS Process Flow

1. Create n-well regions and channel-stop regions
2. Grow field oxide and gate oxide (thin oxide)
3. Deposit and pattern polysilicon layer
4. Implant source and drain regions, substrate contacts
5. Create contact windows, deposit and pattern metal layer
Lithography Masks

- Each lithography step during fabrication must be defined by a separate lithography mask.

- Each mask layer is drawn (either manually or using a design automation tool) according to the layout design rules.

- The combination (superposition) of all necessary mask layers completely defines the circuit to be fabricated.
active
poly
implant
contacts
metal
Composite Mask Layout
Layout Design Rules

- To allow reliable fabrication of each structure, the mask layers must conform to a set of geometric layout design rules.

- Usually, the rules (for example: minimum distance and/or separation between layers) are expressed as multiples of a scaling factor – lambda (λ).

- For each different fabrication technology, lambda factor can be different.
3D Perspective

Polysilicon

Aluminum

Gate Oxide

Field Oxide

Source / Drain Regions

P-Type

Field Oxide
## CMOS Process Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td></td>
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Layers in 0.25 µm CMOS process

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
<td>m1, m2, m3, m4, m5</td>
</tr>
<tr>
<td>well</td>
<td>nw</td>
</tr>
<tr>
<td>polysilicon</td>
<td>poly</td>
</tr>
<tr>
<td>contacts &amp; vias</td>
<td>ct, v12, v23, v34, v45, nwc, pwc</td>
</tr>
<tr>
<td>active area and FETs</td>
<td>ndif, pdif, nfct, pfct</td>
</tr>
<tr>
<td>select</td>
<td>nplus, pplus, prb</td>
</tr>
</tbody>
</table>

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Intra-Layer Design Rules
Design Rule Checker

poly_not_fet to all_diff minimum spacing = 0.14 um.
Layout Design Rules
Layout Rules of a Minimum-Size MOSFET
State-of-the-Art Examples

Source: Nikkei Microdevices 9/02

(a) 90nm ノード向けトランジスタ
Multi-Level Interconnect with CMP
Multi-Level Metal Interconnect

TSMC
0.13μ
8 layers
Cu

(b) 0.13 μmプロセスで製造した
8層Cu配線

Source:
Nikkei
Microdevices
11/00
Multi-Level Metal Interconnect

Source: Nikkei Microdevices 9/02

(b) 90nm ノード向け多層配線
Multi-Level Metal Interconnect
Silicon on Insulator (SOI)

The key innovation in SOI is to build the transistor structures on an **insulating** material rather than a common substrate as in CMOS. This reduces parasitic capacitances and eliminates substrate noise coupling.
Lithography Resolution is Decreasing

With each new technology generation, we would be able to fit the same amount of functionality into a smaller silicon area (ideally).
Lithography Resolution is Decreasing

But at the same time, we try to put more functionality in each chip for each new technology generation, so that the average chip size actually increases over the years!
Final Remark: Fabrication Cost

Initial investment costs of a new fabrication facility