Introduction to VLSI Design

Yu-Min Lee
Assistant Professor
Department of Communication Engineering
National Chiao Tung University
Administrative Matters

- **Time/Location:**
  - Tuesday 15:40~16:30/ED824
  - Thursday 10:10~12:00/ED801
- **Instructor:** Yu-Min Lee
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- **Phone:** 03-5712121 ext 54334
- **URL:** http://vlsi-eda.cm.nctu.edu.tw
- **Office:** ED835
- **Teaching Assistant:**
  - Ahe-Yu Lin (dirker.cm93g@nctu.edu.tw)
  - Jia-Hong Wu (wwjjhh56@hotmail.com)
  - Office: ED718
  - Phone: 03-5712121 ext 54586
- **Prerequisite:** Logic design, Circuit analysis, Basic solid state concepts and models
Administrative Matters


- References:
  - Neil H. E. Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective, 3rd Edition*

- CAD tools:
  - H-Spice: Circuit Simulation
  - Virtuoso: Layout Editor
  - Calibre: DRC
Course Contents

- Introduction, Fabrication, and Layout
- MOS Devices
- MOS Inverters: Static and Dynamic Characteristics
- Interconnect Parasitics
- MOS Logic Circuits
- Dynamic MOS Logic Circuits
- Memories
- Low-Power CMOS Logic Circuits
- Chip Input and Output (I/O) Circuits
- Design for Manufacturability and Testability
**Grading Policy**

- **Grading:**
  - Homework Assignments: 15%
  - Labs: 20%
  - Midterm: 30% (in-class with an A4-size and one-sided page sheet)
  - Final: 35% (in-class with an A4-size and one-sided page sheet)

- **Course Web Site:**
  
  http://vlsi-eda.cm.nctu.edu.tw/vlsi06s.htm

- **Academic Honesty:** Avoiding cheating at all cost.
CMOS Digital Integrated Circuits

Lec 1
Introduction
Some History

Invention of the transistor (BJT) 1947
Shockley, Bardeen, Brattain – Bell Labs

Single-transistor integrated circuit 1958
Jack Kilby – Texas Instruments

Invention of CMOS logic gates 1963
Wanlass & Sah – Fairchild Semiconductor

First microprocessor (Intel 4004) 1970
2,300 MOS transistors, 740 kHz clock frequency

Very Large Scale Integration 1978
Chips with more than ~20,000 devices
More Recently

Ultra Large Scale Integration

System on Chip (SoC)

20 ~ 30 million transistors in 2002

The chip complexity has increased by a factor of 1000 since its first introduction, but the term VLSI remained virtually universal to denote digital integrated systems with high complexity.
Why VLSI?

- Integration improves the design
  - Compactness: less area, physically smaller
  - Higher speed: lower parasitics (reduced interconnection length)
  - Lower power consumption
  - Higher reliability: improved on-chip interconnects

- Integration significantly reduces manufacturing cost
As a result of the continuously increasing integration density and decreasing unit costs, the semiconductor industry has been one of the fastest growing sectors in the worldwide economy.
Industry Trends

Large
Centralized
Expensive

Small / Portable
Distributed
Inexpensive
Industry Trends

High performance
Low power dissipation
Wireless capability
etc…

More portable, wearable, and more powerful devices for ubiquitous and pervasive computing…
Some Leading-Edge Examples

- Intel Pentium 4
- 0.13μm process
- 55 million transistors
- 2.4GHz clock
- 145mm²
Some Leading-Edge Examples

IBM S/390 Microprocessor
0.13 µm CMOS process
7 layers Cu interconnect
47 million transistors
1 GHz clock
180 mm²
Evolution of Minimum Feature Size

![Graph showing the evolution of minimum feature size from 1975 to 2000. The feature size decreases significantly over time.](image)
Evolution of Minimum Feature Size

2002: 130 nm
2003: 90 nm
...
2010: 35 nm (?)
Moore’s Law

- Memory (rate of increase = x 1.5 / year)
- Microprocessor (rate of increase = x 1.25 / year)

Source: Intel Corp.
Evolution of Memory Capacity
## ITRS - International Technology Roadmap for Semiconductors

![ITRS - International Technology Roadmap for Semiconductors](http://public.itrs.net)

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>TECHNOLOGY</td>
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<tr>
<td>DRAM CAPACITY</td>
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Predictions of the worldwide semiconductor / IC industry about its own future prospects...
## Shrinking Device Dimensions

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### Increasing Function Density

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### Increasing Clock Frequency

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### Decreasing Supply Voltage

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Evolution in Power Density

Power Density [W/cm²]


Source: adapted from Intel

CMOS Digital Integrated Circuits
5-layer cross-section of chip
System-on-Chip

Integrating all or most of the components of a hybrid system on a single substrate (silicon or MCM), rather than building a conventional printed circuit board.

1. More compact system realization
2. Higher speed / performance
   • Better reliability
   • Less expensive!
New Direction: System-on-Chip (SoC)
Products have a shorter life-cycle!
longer design time for better performance in current generation

Design

missed technology window = lower performance in next generation

Design

Production

Design

Production

Technology Window 1

Technology Window 2
Better strategy

longer design time for better performance in current generation

missed technology window = lower performance in next generation
The Y-Chart

Notice: There is a need for structured design methodologies to handle the high level of complexity!
Simplified VLSI Design Flow

Top-down

Bottom-up
Top-down vs. bottom-up design

- Top-down design adds functional detail.
  - Create lower levels of abstraction from upper levels.

- Bottom-up design creates abstractions from low-level behavior.

- Good design needs both top-down and bottom-up efforts.
VLSI Design Cycle

System Specification → Architectural Design → Functional Design

- Behavioral VHDL, C

Packing & Testing → Fabrication → Physical Design → Circuit Design

- Logic Design
- Structural VHDL

Figs. [©Sherwani]
VLSI Design Cycle

System Specification
- A high level representation of the system
- Considered factors
  » Performance
  » Functionality
  » Physical dimensions (die size)
- Result Specs – size, speed, power, and functionality

CMOS Digital Integrated Circuits
VLSI Design Cycle

- **Architectural Design**
  - RISC (Reduced Instruction Set Computer) versus CISC (Complex Instruction Set Computer)
  - Number of ALUs, Floating Point Units
  - Number and structure of pipelines
  - Cache size
  - Prediction on die size, power, and speed based on existing design
  - Early estimation are very important here
VLSI Design Cycle

■ Behavioral or Functional Design
  – Only behavior and timing without implementation issue
  – Specify behavior based on Input + output + timing
  – Fast emulation and debugging for the system

always @(posedge clk);
begin
  if (enable_ == 1'b0)
    data = 0;
  else
    data = data + 1;
end
VLSI Design Cycle

Logic Design
– Control flow, word widths, register allocation, arithmetic operations, and logic operations
– RTL (Register Transfer Level) – HDL (Hardware Description Language)
  » Verilog – most popular
  » VHDL – Europe and Eastern
  » Literal + Timing Information

X = (AB*CD) + (A+D)
Y = (A(B+C) + AC+D)

Boolean Expression
Timing Information
VLSI Design Cycle

- Logic Design
  - More actual simulation and testing

- High Level Synthesis: Produce a RTL description from a behavioral description of the design

![Logic Circuit Diagram]
VLSI Design Cycle

- **Circuit Design**
  - Boolean Expression $\rightarrow$ Circuit Elements (Cells, Macros, Gates, Transistors) + Interconnection
  - Each component has specific timing and power Info.
  - Circuit Simulation: Verify the correctness and timing
  - Terms – Netlist, Schematic
  - Logic Synthesis Tools: RTL $\rightarrow$ Netlist
VLSI Design Cycle

- Physical Design
  - Netlist → Layout (Geometry Representation)
    » Design rules of applied fabrication process
  - Layout Synthesis Tools
    » Automatic conversion (Fully/Partially)
    » Area and performance penalty
  - Crucial Challenges – Area/Delay
VLSI Design Cycle

- **Fabrication**
  - Layout → Photo-lithographic mask
    - One mask for each layer
  - Wafer: Silicon crystal are grown & sliced
  - Deposition, and diffusion of various materials on the wafer: each step uses one mask
  - Term: Tape Out, 8 inch/20cm, 12 inch/30cm
VLSI Design Cycle

- Packaging, Testing, and Debugging
  - For PCB (Printed Circuit Board): DIP (Dual In-line Package), PGA (Pin Grid Array), BGA (Ball Grid Array), and QFP (Quad Flat Package)
  - For MCM (Multi-Chip Modules): no packaged
  - Testing
    » Before Package – Probe line testing
    » After Package – Tester machine applies test patterns.
Structured Design Principles

Hierarchy: “Divide and conquer” technique involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.

Regularity: The hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible. Regularity usually reduces the number of different modules that need to be designed and verified, at all levels of abstraction.

Modularity: The various functional blocks which make up the larger system must have well-defined functions and interfaces.

Locality: Internal details remain at the local level. The concept of locality also ensures that connections are mostly between neighboring modules, avoiding long-distance connections as much as possible.
Hierarchy of a 4-bit Carry Ripple Adder
Hierarchy of a 16-bit Manchester Adder
Hierarchy of a 16-bit Manchester Adder

16-bit adder complete layout
Hierarchy of a 16-bit Manchester Adder

4-bit adder with Manchester carry
Hierarchy of a 16-bit Manchester Adder

Carry/propagate circuit layout

Manchester carry circuit layout

Output buffer/latch circuit layout
Regularity

2-input MUX

DFF
VLSI Design Styles

- Full-custom
- Semi-custom
  - Masked gate array (MGA)
  - Cell-based (CBIC) (standard cells)
- Programmable
  - PLD
  - CPLD
  - FPGA
Following the partitioning, the transistor level design of the building block is generated and simulated.

The example shows a 1-bit full-adder schematic and its SPICE simulation results.
Full Custom Design

The main objective of full custom design is to ensure fine-grained regularity and modularity.
Full Custom Design

A carefully crafted full custom block can be placed both along the X and Y axis to form an interconnected two-dimensional array.

Example:

Data-path cells
Full Custom SRAM Cell Design
Mapping the Design into Layout

Manual full-custom design can be very challenging and time consuming, especially if the low level regularity is not well defined!
VLSI Design Styles

- Full-custom
- Semi-custom
  - Masked gate array (MGA)
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HDL-Based Design

1980’s
Hardware Description Languages (HDL) were conceived to facilitate the information exchange between design groups.

1990’s
The increasing computation power led to the introduction of logic synthesizers that can translate the description in HDL into a synthesized gate-level net-list of the design.

2000’s
Modern synthesis algorithms can optimize a digital design and explore different alternatives to identify the design that best meets the requirements.
HDL-Based Design

The design is synthesized and mapped into the target technology.

The logic gates have one-to-one equivalents as standard cells in the target technology.
Standard Cells

Library Construction

- To enable automated placement of the cells and routing of inter-cell connections, each cell layout is designed with a fixed height, so that a number of cells can be abutted side-by-side to form rows.
Standard Cells
Standard Cells

After chip logic design being done by using standard cells from the library

- Place the individual cells into rows
- Interconnect them that meets the design goal in circuit speed, chip area and power consumption.
Standard Cells

Rows of standard cells with routing channels between them

Memory array
Standard Cells
VLSI Design Styles

- Full-custom
- Semi-custom
  - Cell-based (CBIC) (standard cells)
  - Masked gate array (MGA)
- Programmable
  - PLD
  - CPLD
  - FPGA
Mask Gate Array

- Metal mask design and processing
- Chip utilization factor is higher than the FPGA and so is speed.
- Number of gates: hundreds of thousands of logic gates
Mask Gate Array-Sea of Gate

Before customization
VLSI Design Styles

- Full-custom
- Semi-custom
  - Cell-based (CBIC) (standard cells)
  - Masked gate array (MGA)
- Programmable
  - PLD
  - CPLD
  - FPGA
Field Programmable Gate Array: FPGA

- User programming
- Very short turn around time
- Price is higher than standard cell and mask gate array.
- Number of gates: 25,000 ~ 20,000 gates
Field Programmable Gate Array

Internal structure of a CLB

© CMOS Digital Integrated Circuits – 3rd Edition
Field Programmable Gate Array

Six Pass Transistors Per Switch Matrix Interconnect Point
## International Technology Roadmap for Semiconductors (ITRS’03)

<table>
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<tr>
<th>Technology (nm)</th>
<th>hp90</th>
<th>hp65</th>
<th>hp45</th>
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<th>hp22</th>
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<td>154</td>
<td>309</td>
<td>617</td>
<td>1235</td>
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<td>9,285</td>
<td>15,079</td>
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<td>39,683</td>
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<tr>
<td>Area (mm²)</td>
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<td>310</td>
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<tr>
<td>#metal levels</td>
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<td>11</td>
<td>12</td>
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