Modeling and Optimization of VLSI Interconnects

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Administrative Matters

- Lecture Time: **18:30~21:20 Tuesday**
- Lecture Location: **ED103**
- Instructor: **Yu-Min Lee**
- Office: **ED835**
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- E-mail: **yumin@nctu.edu.tw**
- Office Hour: **13:30~14:30 Tuesday**
- URL: [http://vlsi-eda.cm.nctu.edu.tw/course/Interconnect_11Spring/lecture.html](http://vlsi-eda.cm.nctu.edu.tw/course/Interconnect_11Spring/lecture.html)
- TA: **Shu-Han Wei**
  - Office- **ED718**
  - Phone- **54586**
  - E-mail- [littlelittle821@gmail.com](mailto:littlelittle821@gmail.com)

Prerequisites: **Mainly self-contained**
Text/Reference Material

- Cong et al., *Performance Optimization of VLSI Interconnect Layout*, Integration, the VLSI Journal 21, 1996 1--94.
- Selected research papers from IEEE TCAD, ACM TODAES, and major CAD conference such as DAC, ICCAD, ISPD, and DATE.
Course Contents

- Course Objectives
  - Present a broad survey of the problems in modeling and design of high-performance VLSI interconnect and state of art solutions. Provide necessary background for graduate students to carry out research in this area.

- Course Contents
  - Overview and Introduction
  - Modeling of VLSI Interconnects
  - *Introduction to Parasitic Extraction*
  - Interconnect Delay Modeling & Calculation
  - Interconnect Sizing
  - Introduction of Noise Modeling and Reduction
  - Power Delivery Network Analysis and Design
  - Thermal Modeling and Analysis
  - *Clock Network Design*
  - Presentation of Paper Survey
  - Preparation & Presentation of Project
Grading Policy

- Homework Assignments: 20%
- Paper Survey: 25%
- Project: 30% (1 person per group)
- Midterm (Take Home Exam): 25%
- Academic Honesty: Avoiding cheating at all cost.

3/20 before determining the topic (with instructor approval): Late one day, deduct 1 point from the final grade, and so on.
- Topic should be relevant and approved by the instructor; some reference topics include:
  1) Parasitic Extraction
  2) Delay Modeling & Calculation Related Topics
  3) Interconnect Noise Modeling & Reduction Related Topics
  4) Power Delivery Network Related Topics
  5) Thermal Modeling, Simulation and Thermal-Aware Design Related Topics
  6) Clock Network Design Related Topics
  7) Model Order Reduction Techniques
- Paper Report – 15%
  - Report has a fixed format (see course website). Main text (excluding charts, references) page count must be at least 10 pages.
- Presentation – 10%
  - Report document page count must be at least 25 pages. Report time must be at least 30 minutes.

Avoid cheating at all cost.